Designing Reliable and Low Power Multiplier by using Algorithmic Noise Tolerant

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Abstract—This paper, proposes an area efficient multiplier design using fixed-width replica redundancy by adopting Algorithmic Noise Tolerant (ANT) architecture. The fixed-width multiplier is used to build the reduced precision replica redundancy block (RPR). The proposed ANT design can take care of the demand of high exactness, low power consumption, and area efficiency. It is designed with the fixed-width RPR with error compensation circuit by means of breaking down of likelihood and measurements. Using the partial product terms of input correction vector and minor in-put correction vector to lower the truncation errors, the equipment many-sided quality of error compensation circuit can be disentangled, circuit area in our fixed-width RPR can be lower and power consumption in our ANT design can be saved as compared with the existing ANT design.

Keywords— Algorithmic noise tolerant (ANT), reduced-precision replica (RPR), voltage over scaling(VOS), Main Digital Signal Processing (MDSP).

I. INTRODUCTION

The rapid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To bring down the force dissemination, supply voltage scaling is broadly utilized as a successful low-control strategy since the force utilization in CMOS circuits is corresponding to the square of supply voltage. Notwithstanding, in profound sub micrometer process innovations, clamor obstruction issues have raised trouble to outline the dependable and productive microelectronics frameworks; thus, the configuration strategies to improve commotion resistance have been generally created.

This project proposes a reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT engineering can take care of the demand of high exactness, low power utilization, and zone effectiveness. Outlining the settled width RPR by utilizing the altered Wallace tree multiplier; an error compensated adder tree is constructed in order to round off truncation errors. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. An aggressive low power technique, referred to as voltage over scaling (VOS), was proposed in lower supply volt–age past basic supply voltage, without relinquishing the throughput. However, VOS prompts serious corruption in signal-to-noise ratio (SNR). A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced-precision replica (RPR), which battles delicate blunders viably while accomplishing noteworthy vitality sparing. Some ANT misshaping plans are exhibited in the ANT outline idea is further stretched out to framework level. Be that as it may, the RPR outlines in the ANT are in a tweaked way, which are not effortlessly received and rehashed.

II. RELATED WORK

The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex as shown in Fig.1. As a result, the RPR design in the ANT design is still the most prevalent configuration in view of its effortlessness. However, adopting with RPR should still pay extra area overhead and power consumption. In this paper, it is further proposed an easy way using the fixed-width RPR to replace the full-width RPR block. Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. The use of probability, statistics, and partial product weight analysis to find the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, it is restrict the compensation circuit in RPR must not be located in the critical path.
Fig.1: ANT architecture.


In this paper, an energy-efficient soft error-tolerant techniques for digital signal processing (DSP) systems is referred to as algorithmic soft error-tolerance (ASET), employs low-complexity estimators of a main DSP block to achieve reliable operation in the presence of soft errors. Three distinct ASET techniques—spatial, temporal and spatio-temporal—are presented. For frequency selective finite-impulse response (FIR) filtering, it is shown that the proposed techniques provide robustness in the presence of soft error. For a range of sampling frequencies, the proposed technique provides robustness in the presence of soft error rates of up to $er = 10^{-2}$ and $er = 10^{-3}$ in a single-event upset scenario. The power dissipation of the proposed techniques ranges from 1.1X to 1.7X (spatial ASET) and 1.05X to 1.17X (spatio-temporal and temporal ASET) when the desired signal-to-noise ratio $SNR_{des} = 25$dB. In comparison, the power dissipation of the commonly employed triple modular redundancy technique is 2.9X.


In this paper, a framework for low-energy digital signal processing (DSP) where the supply voltage is scaled beyond the critical voltage required to match the critical path delay to the throughput. This deliberate introduction of input-dependent errors leads to degradation in the algorithmic performance, which is compensated for via algorithmic noise-tolerance (ANT) schemes. The resulting setup that comprises of the DSP architecture operating at sub-critical voltage and the error control scheme is referred to as soft DSP. It is shown that technology scaling renders the proposed scheme more effective as the delay penalty suffered due to voltage scaling reduces due to short channel effects. The effectiveness of the proposed scheme is also enhanced when arithmetic units with a higher “delay-imbalance” are employed. A prediction based error-control scheme is proposed to enhance the performance of the filtering algorithm in presence of errors due to soft computations. For a frequency selective filter, it is shown that the proposed scheme provides 60% - 81% reduction in energy dissipation for filter bandwidths up to 0.5X, which corresponds to the sampling frequency $f_s$ over thus achieved via conventional voltage scaling, with a maximum of 0.5dB degradation in the output signal-to-noise ratio ($SNR_{out}$). It is also shown that the proposed algorithmic noise-tolerance schemes can be used to improve the performance of DSP algorithms in presence of bit-error rates of up to $10^{-3}$ due to deep submicron (DSM) noise.

III. PROPOSED ANT MULTIPLIER DESIGN US-ING FIXED-WIDTH RPR

In this paper, it is further proposed that fixed-width RPR to replace the full-width RPR block in the ANT design [2], as shown in Fig.2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. It demonstrate our fixed-width RPR-based ANT design in an ANT multiplier. The disadvantages of existing system are, RPR designs in the ANT designs are designed in a customized manner, which are not easily adopted and repeated, their hardware complexity is too complex. It still pays extra area overhead and power consumption

The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely. Many literatures have been presented to reduce the truncation error with constant correction value with variable correction value. The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise, their compensation method is to compensate the truncation error between the full-length multiplier and the fixed-width multiplier. However, in the fixed-width RPR of an ANT multiplier, the compensation error we need to correct is the overall truncation error of MDSP block. Unlike, our compensation method is to compensate the truncation error between the full-length MDSP multiplier and the fixed-width RPR multiplier.

The objective of this project is to propose a fixed-width RPR to replace the full-width RPR block in the ANT design, which not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture.
The ANT technique [2] includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay $T_{cp}$ of the system becomes greater than the sampling period $T_{samp}$, the soft errors will occur. It leads to severe degradation in signal precision.

The error correction hunk which consist of multiplexer, RPR block compensation circuits and registers. In error correction block the inputs are given to the RPR block. The function of the RPR block is to correct the errors occurring in the output. The RPR hunk take the input as partial products. If the input is 12x12 bits it takes half of the partial terms or MSB segments. The RPR only takes 6 bits for processing. Error in the output is minimized or truncated. After that the compensation circuit to compensate the truncated errors and finally produce the input we use RPR method. Mutually the outputs are taken to the decision block. This hunk is used for selecting the error free output. With the help of selection line the multiplier choose the correct output. The variable precision value is used to achieve good precision value. The input correction vector is used in error compensation circuit for compensating the errors. The error in the output is minimized.

In the ANT technique [2], a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output $ya[n]$; however, RPR output $yr[n]$ is still correct since the critical path delay of the replica is smaller than $T_{samp}$ [4]. Therefore, $yr[n]$ is applied to detect errors in the MDSP output $ya[n]$. Error detection is accomplished by comparing the difference $|ya[n] - yr[n]|$ against a threshold $Th$. Once the difference between $ya[n]$ and $yr[n]$ is larger than $Th$, the output $yr[n]$ is applied to compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the non-critical path of the fixed-width RPR. As compared with the full-width RPR design in, the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

Fig. 3: 12 × 12 bit ANT multiplier is implemented with the six-bit fixed width replica redundancy block.

There are many fixed-width multiplier designs applied to the full-width multipliers. However, there is still no fixed-width RPR design applied to the ANT multiplier designs. To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm makes use of probability, statistics, and linear regression analysis to find the approximate compensation value.

To save hardware complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates. To further lower the compensation error, we also consider the impact of truncated products with the second most significant bits on the error compensation. We propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the non-critical path of the fixed-width RPR. As compared with the full-width RPR design in, the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

B. Applications

The proposed method is more efficient compared to existing method and the Audio and speech signal processing, sonar and radar signal processing, sensor array processing, spectral estimation, statistical signal processing. Digital image processing, signal processing for communications, control of systems, biomedical signal processing, seismic data processing, multimedia applications and Filters.

A. Advantages

Proposed method advantages are, higher computation precision, lower power consumption, lower area overhead in RPR. Perform with higher SNR, lower operating supply voltage, lower power consumption.
IV. RESULTS AND DISCUSSION

In this zone, we converse about the concert of the proposed RPR ANT structure. First, we define the main block, it is simulated by using MODELSIM software. Here two inputs are x and y.

Second, we define the EC block, error correction block is simulated by using MODELSIM software.

In order to evaluate the performance of design, we have to compare the performance of this fixed width RPR design with previous full width RPR design. The design is synthesized by using Xilinx 8.1V.

In this zone to determine the optimized bit-length of fixed-RPR, comparisons of the Kvos and RPR area with different bit length of RPR block are shown in Fig. 4. Our goal is to select the bit length of fixed-RPR, which can achieve the lowest Kvos. The smaller RPR can perform with higher speed, lower power consumption and lower area.

The RPR area is another key factor that will affect the power saving. Hence, we compare the circuitry area occupied by the fixed-width RPR multiplier and the full-width RPR multiplier.

The total synthesized logic cell silicon area for various RPR designs is plotted in Fig. 5. As illustration, the silicon area in the proposed design can be averagely saved by 45.51% as compared with various word length full-width RPR multiplier.
designs. Under the case of six-bit fixed-width RPR multiplier design, the chip area occupied by total logic cells can be saved by 44.55% as compared with the six-bit full-width RPR design. Comparison is as shown in the table.

<table>
<thead>
<tr>
<th>Functions</th>
<th>Existing method</th>
<th>Proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time delay</td>
<td>41.488ns</td>
<td>10.032ns</td>
</tr>
<tr>
<td>Area</td>
<td>5145</td>
<td>750</td>
</tr>
<tr>
<td>Power</td>
<td>97mW</td>
<td>23mW</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

In this paper, the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 VDD, and power consumption in our ANT design can be saved by 23% as compared with the existing system.

Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. We take use of probability, statistics, and partial product weight analysis to find the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

REFERENCES